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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,012	02/11/2004	Richard W. Foote	P05792	3404

23990 7590 02/18/2009

DOCKET CLERK
P.O. DRAWER 800889
DALLAS, TX 75380

EXAMINER	
FULK, STEVEN J	
ART UNIT	PAPER NUMBER
2891	

MAIL DATE	DELIVERY MODE
02/18/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,012	FOOTE ET AL.	
	Examiner	Art Unit	
	STEVEN J. FULK	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-10,13-17 and 20-42* is/are pending in the application.

4a) Of the above claim(s) *22-42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-10,13-17,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 7, 8, 10, 13-17 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Matthews '945 (previously cited).

Where product-by-process limitations are recited, the claims are limited only by the structure implied by the steps, not the manipulations of the steps. For example, anticipation of claim 7 does not require that the doping be performed by implantation (in-situ doping would result in the same structure); anticipation of claim 7, 13, or 16 does not require the doping to be performed simultaneously; anticipation of claim 17 does not require etching to separate the source and drain (masked deposition would result in the same structure).

Regarding claims 1, 2 and 4, Matthews discloses a semiconductor apparatus comprising at least one NPN double poly bipolar transistor (fig. 13B, NPN transistor 20) and at least one PMOS double poly metal oxide semiconductor transistor (fig. 13A, P-channel FET 40), wherein a base of the double poly bipolar transistor (fig. 14B, base 35) and a gate of the double poly metal oxide semiconductor transistor (fig. 14A, gate 33) contain substantially identical dopants concentrations (polysilicon of base 35 and gate 33 is simultaneously doped by implant 42, thus having identical dopant species

and concentration; col. 14, lines 44-50); wherein the at least one double poly bipolar transistor and the at least one double poly metal oxide semiconductor transistor comprise a substrate (fig. 7A/B, substrate 10) and a first layer of polysilicon material (31); wherein the apparatus comprises a first polysilicon layer in the at least one double poly bipolar transistor that is doped with impurity ions to form an extrinsic base (fig. 14B, 35); and the first layer of polysilicon material in the at least one double poly MOS transistor is doped with impurity ions to form an MOS transistor gate (fig. 14A, 33); and further comprising a second layer of polysilicon material (figs. 11A/B, 58) that is separate from the first polysilicon layer.

Regarding claims 7, 8 and 10, the reference discloses the substrate is implanted with impurity ions to form an intrinsic base (fig 10B, 50) in the at least one double poly bipolar transistor; and the substrate is simultaneously implanted with impurity ions to form a self-aligned lightly doped drain (fig. 10A, 53/54; col. 12, lines 30-56) in the at least one double poly MOS transistor.

Regarding claims 13-15, 17 and 20, the reference discloses the at least one double poly bipolar transistor and the at least one double poly metal oxide semiconductor transistor further comprise a second layer of polysilicon material (figs. 11A/B, 58); wherein the second layer of polysilicon material in the at least one double poly bipolar transistor is doped with impurity ions to form a self-aligned emitter (fig. 13B, 67); and the second layer of polysilicon material in the at least one double poly MOS transistor is doped with impurity ions to form a self-aligned MOS source/drain (fig. 13A, 68/69).

Regarding claim 16, the reference discloses the second layer of polysilicon material in the at least one double poly bipolar transistor is doped with impurity ions to form a deep collector (fig. 15B, 84).

3. Claims 1-3, 7, 9, 13 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Maeda et al. '760 (previously cited).

Regarding claims 1-3, Maeda discloses a semiconductor apparatus comprising a substrate (fig. 1G, 10), at least one PNP double poly bipolar transistor that comprises a first polysilicon layer doped with impurity ions to form an extrinsic base (figs. 1G & 1H, PNP device with base in first poly layer 58 and emitter in second poly layer 37) and at least one NMOS double poly metal oxide semiconductor transistor with a first layer of polysilicon material doped with impurity ions to form an MOS transistor gate (figs. 1G &1H, NMOS device with gate in first poly layer 50 and source/drain in second poly layer 39); wherein the base of the double poly bipolar transistor and the gate of the double poly metal oxide semiconductor transistor contain substantially identical dopants concentrations (col. 4, lines 44-48; claims 25 and 26); and further comprising a second layer of polysilicon material (fig. 1H, 37) that is separate from the first polysilicon layer.

Regarding claims 7 and 9, the reference discloses the substrate is implanted with impurity ions to form an intrinsic base (fig. 1G, 57) in the at least one double poly bipolar transistor; and the substrate is implanted with impurity ions to form a self-aligned lightly doped drain (col. 3, lines 43-65) in the at least one double poly MOS transistor.

Regarding claims 13 and 21, the reference discloses the at least one double poly bipolar transistor and the at least one double poly metal oxide semiconductor transistor

further comprise a second layer of polysilicon material; wherein the second layer of polysilicon material in the at least one double poly bipolar transistor is doped with impurity ions to form an emitter (fig. 1H, 37); and the second layer of polysilicon material in the at least one double poly MOS transistor is doped with impurity ions to form a MOS source/drain (fig. 1H, 39).

Response to Arguments

4. Applicant's arguments with respect to claims 1-4, 7-10, 13-17 and 20-21 have been considered but are not found persuasive. Applicant argues that Matthews does not teach a first polysilicon layer and a second polysilicon layer that is separate from the first polysilicon layer. Applicant argues that polysilicon layer 31 is formed from poly layers 26 and 31, and the layers are not separate. Applicant is mischaracterizing the rejection. The Examiner's position is that the first polysilicon layer of Matthews is defined as layer 31 of Fig. 7B. The process of how this layer is formed is irrelevant in the product claim. Layer 31 then forms the base of the double poly bipolar transistor (fig. 14B, base 35) and the gate of the double poly metal oxide semiconductor transistor (fig. 14A, gate 33). The second polysilicon layer of Matthews is defined as layer 58 of Fig. 11A/B, which is separate from the first polysilicon layer 31 by insulating spacers. Layer 58 then forms a self-aligned emitter for the bipolar transistor (fig. 13B, 67) and the MOS source/drain (fig. 13A, 68/69). The language of claim 1 of "a first polysilicon layer and a second silicon layer" (emphasis added) is written broadly enough to be anticipated by any two polysilicon layers of Matthews that form the required structure.

Applicant also argues that Maeda does not teach a first polysilicon layer and a second polysilicon layer that is separate from the first polysilicon layer. Applicant argues that the first polysilicon layer is formed from poly layers 24 and 55, and the layers are not separate. Applicant is mischaracterizing the rejection. The Examiner's position is that the first polysilicon layer of Matthews is defined as layer 55 of Fig. 1F. The process of how this layer is formed is irrelevant in the product claim. Layer 55 then forms the base of the double poly bipolar transistor (fig. 1G, 58) and the gate of the double poly metal oxide semiconductor transistor (fig. 1G). The second polysilicon layer of Matthews is defined as the layer that forms the emitter of the bipolar transistor (fig. 1H, 37) and the extrinsic source/drain of the MOS (39), which is separate from the first polysilicon by insulating spacers. The language of claim 1 of "a first polysilicon layer and a second silicon layer" (emphasis added) is written broadly enough to be anticipated by any two polysilicon layers of Matthews that form the required structure.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN J. FULK whose telephone number is (571)272-8323. The examiner can normally be reached on Monday through Friday, 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven J. Fulk/
Examiner, Art Unit 2891
February 5, 2009

/Douglas M Menz/

Primary Examiner, Art Unit 2891
2/14/09